



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO.	SERIAL NUMBER
	211.001-D2-US	10/724,377
	APPLICANT(S) Fazan et al.	
FILING DATE	GROUP ART UNIT	
November 28, 2003		

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WSL	4,032,947	6/1977	Kesel et al.			
	3,997,799	12/1976	Baker			
	5,448,513	9/1995	Hu et al.			
	4,298,962	11/1981	Hamano et al.			
	3,439,214	4/1969	Kabell			
	6,081,443	6/2000	Morishita			
↓	6,111,778	8/2000	MacDonald et al.			

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WSL	FR 2 197 494	3/1974	French			
	EP 1 180 799	2/2002	European			
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	GB 1 414 228	11/1975	Great Britain			
	EP 0 694 977	1/1996	European			
	JP 02 294076	2/1991	Japanese			
	EP 1 237 193	9/2002	European			
↓	EP 0 878 804	11/1998	European			

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WSL	"The Multistable Charge-Controlled Memory Effect in SOI MOS Transistors at Low Temperatures", Tack et al., IEEE Transactions on Electron Devices, Vol. 37, No. 5, May 1990, pp.1373-1382

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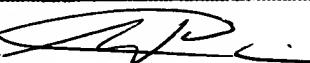
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WSL	5,936,265	8/1999	Koga			
	5,780,906	7/1998	Wu et al.			
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↓	5,696,718	12/1997	Hartmann			

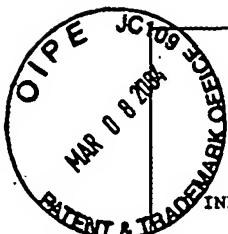
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WSL	EP 0 801 427	10/1997	European			
WSL	EP 0 513 923	11/1992	European			

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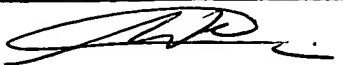
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W&L	4,298,962	11/1981	Hamano et al.			
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	6,518,105	2/2003	Yang et al.			
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W&L	EP 0 731 972	11/2001	European			
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	"The Multistable Charge-Controlled Memory Effect in SOI MOS Transistors at Low Temperatures", Tack et al., IEEE Transactions on Electron Devices, Vol. 37, No. 5, May 1990, pp.1373-1382
✓	"Mechanisms of Charge Modulation in the Floating Body of Triple-Well nMOSFET Capacitor-less DRAMs", Villaret et al., Proceedings of the INFOS 2003, Insulating Films on Semiconductors, 13th Bi-annual Conference, June 18-20, 2003, Barcelona (Spain), (4 pages)

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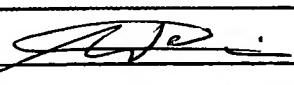
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WSL	2001/0055859	12/2001	Yamada et al.			
	2002/0030214	3/2002	Horiguchi			
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	2002/0051378	5/2002	Ohsawa			
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	2003/0015757	1/2003	Ohsawa			
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W&L	2003/0146488	8/2003	Nagano et al.			
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	6,351,426	2/2002	Ohsawa			
	6,466,511	10/2002	Fujita et al.			
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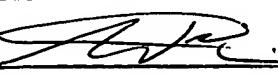
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WSL	4,979,014	12/1990	Hieda et al.			
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wsl	5,886,385	3/1999	Arisumi et al.			
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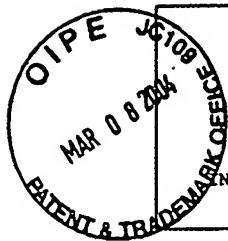
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WSL	6,391,658	5/2002	Gates et al.			

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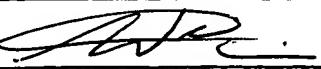
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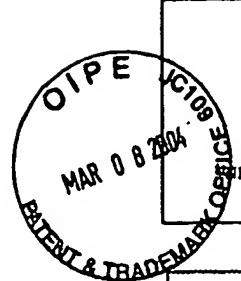
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	"Embedded DRAM Process Technology", M. Yamawaki, Proceedings of the Symposium on Semiconductors and Integrated Circuits Technology, 1998, Vol.55, pp.38-43
↓	"3-Dimensional Simulation of Turn-off Current in Partially Depleted SOI MOSFETs", Ikeda et al., IEIC Technical Report, Institute of Electronics, Information and Communication Engineers, 1998, Vol. 97, No. 557 (SDM97 186-198), pp.27-34

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	211.001-D2-US	10/724,377
	APPLICANT(S) Fazan et al.	
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W/S	EP 1 288 955 A2	3/2003	European			
	EP 1 280 205 A2	1/2003	European			
	EP 1 253 634 A2	10/2002	European			
	EP 1 241 708 A2	9/2002	European			
	EP 1 209 747 A2	5/2002	European			
	EP 1 204 147 A1	5/2002	European			
	EP 1 204 146 A1	5/2002	European			
	EP 1 179 850 A2	2/2002	European			
	EP 1 162 744 A1	12/2001	European			
	EP 1 162 663 A2	12/2001	European			
	EP 1 073 121 A2	1/2001	European			
	EP 0 993 037 A2	4/2000	European			
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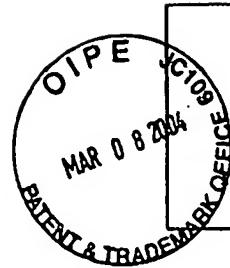
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	EP 0 924 766 A2	6/1999	European			
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	EP 0 860 878 A2	8/1998	European			
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	EP 0 744 772 B1	8/2002	European			
	EP 0 739 097 A2	10/1996	European			
✓	EP 0 731 972 B1	11/2001	European			
✓	EP 0 727 822 B1	8/1999	European			

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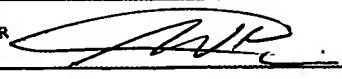
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	EP 0 725 402 B1	9/2002	European			
	EP 0 689 252 B1	8/2000	European			
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	EP 0 642 173 A1	3/1995	European			
	EP 0 606 758 B1	9/2000	European			
	EP 0 601 590 B1	4/2000	European			
	EP 0 599 506 A1	6/1994	European			
	EP 0 599 388 B1	8/2000	European			
	EP 0 579 566 A2	1/1994	European			
	EP 0 564 204 A2	10/1993	European			
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WLR	EP 0 510 607 B1	2/1998	European			
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	EP 0 366 882 B1	5/1995	European			
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	EP 0 333 426 B1	7/1996	European			
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	EP 0 253 631 B1	4/1992	European			
	EP 0 245 515 B1	4/1997	European			
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✓	EP 0 175 378 B1	11/1991	European			

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WSL	2002/0036322	3/2002	Divakauni et al.			
	5,446,299	8/1995	Acovic et al.			
	5,568,356	10/1996	Schwartz			
	5,627,092	5/1997	Alsmeier et al.			
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	5,740,099	4/1998	Tanigawa			
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	5,930,648	7/1999	Yang			
	5,939,745	8/1999	Park et al.			
	5,943,258	8/1999	Houston et al.			
	5,968,840	10/1999	Park et al.			
✓	5,977,578	11/1999	Tang			
✓	6,018,172	1/2000	Hidada et al.			

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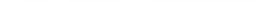
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION Y/N
YSL	JP 62 272561	11/1987	Japanese			
↓	JP 8 274277	10/1996	Japanese			
↓	JP 9 82912	3/1997	Japanese			

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Other Securities (including stocks, bonds, notes, warrants, etc.)

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WSL	2002/0064913	5/2002	Adkisson et al.			
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	2002/0086463	7/2002	Houston et al.			
	2002/0089038	7/2002	Ning			
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	4,791,610	12/1988	Takemae			
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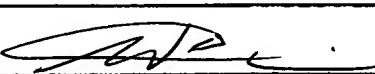
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1082	5,778,243	7/1998	Aipperspach et al.			
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	5,943,258	8/1999	Houston et al.			
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	6,171,923	1/2001	Chi et al.			
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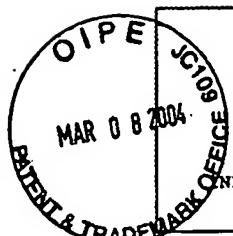
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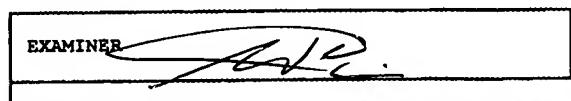
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✓/62	6,214,694	4/2001	Leobandung et al.			
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	6,429,477	8/2002	Mandelman et al.			
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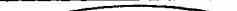
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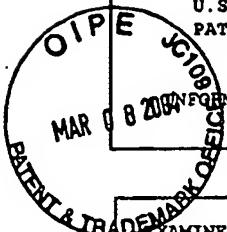
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION FILE NO
WSL	JP 11 87649	3/1999	Japanese			

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	2002-246571	8/2002	Japanese			
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	2002-343886	11/2002	Japanese			
	2002-353080	12/2002	Japanese			
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WSL	DRAM Design Using the Taper-Isolated Dynamic RAM Cell, Leiss et al., IEEE Transactions on Electron Devices, Vol. ED-29, No. 4, April 1982, pp707-714

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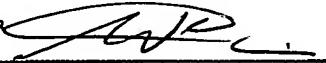
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	2003-132682	5/2003	Japanese			
	2003-203967	7/2003	Japanese			
	2003-243528	8/2003	Japanese			
	09046688	2/1997	Japanese			
✓	JP 8-213624	8/1996	Japanese			
✓	JP 3-171768	7/1991	Japanese			

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